

NX5L2750C

Analog switch with negative swing audio capability

Rev. 1 — 6 September 2013

Product data sheet

1. General description

The NX5L2750C is a dual low-ohmic single-pole double-throw analog switch suitable for use as an analog or digital 2 : 1 multiplexer/demultiplexer. Each switch has a digital select input (nS), two independent inputs/outputs (nY_0 and nY_1) and a common input/output (nZ).

The NX5L2750C is capable of switching audio signals with negative swing without the need of a coupling capacitor.

Schmitt trigger action at the digital inputs makes the circuit tolerant to slower input rise and fall times. Low threshold digital inputs allows this device to be driven by 1.8 V logic levels in 3.3 V applications without significant increase in supply current I_{CC} . This makes it possible for the NX5L2750C to switch 5 V audio signals with a 1.8 V digital controller, eliminating the need for logic level translation.

2. Features and benefits

- Supply voltage range from 1.8 V to 5.0 V
- 0.8 Ω typical ON resistance
- 100 MHz typical bandwidth or data frequency
- CMOS low-power consumption
- 1.8 V control logic at $V_{CC} = 3.6$ V
- Break-before-make switching
- ESD protection:
 - ◆ HBM JESD22-A114F Class 3A exceeds 4000 V
 - ◆ CDM AEC-Q100-011 revision B exceeds 1000 V
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- Specified from -40 °C to $+85$ °C

3. Applications

- Cellular phones, PDA
- Portable media players
- Personal media players



4. Ordering information

Table 1. Ordering information

Type number	Package	Temperature range	Name	Description	Version
NX5L2750CGU	XQFN10	–40 °C to +85 °C		plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.40 × 1.80 × 0.50 mm	SOT1160-1

5. Marking

Table 2. Marking

Type number	Marking code
NX5L2750CGU	LA

6. Functional diagram

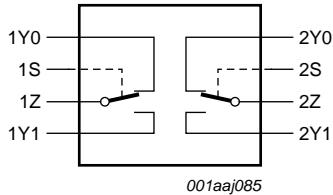
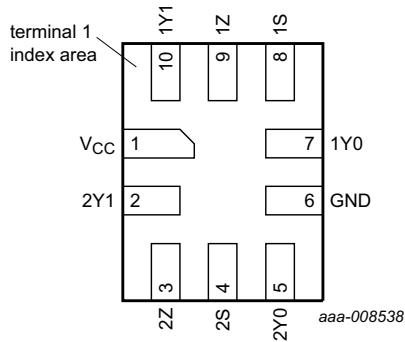


Fig 1. Logic symbol

7. Pinning information

7.1 Pinning



Transparent top view

Fig 2. Pin configuration SOT1160-1 (XQFN10)

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
V _{CC}	1	supply voltage
2Y0, 1Y0	5, 7	independent input or output
2Z, 1Z	3, 9	common output or input
2S, 1S	4, 8	select input
GND	6	ground (0 V)
2Y1, 1Y1	2, 10	independent input or output

8. Functional description

Table 4. Function table^[1]

Input	Channel on
nS	
L	nY0 = nZ
H	nY1 = nZ

[1] H = HIGH voltage level; L = LOW voltage level.

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+5.5	V
V _I	input voltage	pins nS	^[1] -0.5	+5.5	V
V _{SW}	switch voltage		-4.0	V _{CC} + 0.5	V
I _{IK}	input clamping current	V _I < -0.5 V	-50	-	mA
I _{SK}	switch clamping current	V _I < -4.0 V or V _I > V _{CC} + 0.5 V	-	±50	mA
I _{sw}	switch current	T _{amb} = 25 °C	-	±250	mA
		T _{amb} = 25 °C; peak current (pulsed at 1 ms duration; < 10 % duty cycle)	-	±500	mA
I _{CC}	supply current		-	+50	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +85 °C	-	250	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

10. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		1.8	5.0	V
V _I	input voltage	pins nS	0	5.0	V
V _{SW}	switch voltage		[1] -2.5	V _{CC}	V
T _{amb}	ambient temperature		-40	+85	°C

[1] The voltage across the switch should be < 5.5 V.

11. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 2.7 V to 4.3 V	1.4	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.7 V to 4.3 V	-	-	0.6	V
V _{IK}	input clamping voltage	V _{CC} = 3.0 V; I _I = -18 mA	-	-	-1.2	V
I _I	input leakage current	pins nS; V _I = 0 V to V _{CC} ; V _{CC} = 0 V to 4.3 V	-	-	±1	μA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 2.7 V; V _I = -2.5 V or 2.5 V; V _O = 2.5 V or -2.5 V; see Figure 3	-	-	±250	nA
I _{CC}	supply current	V _I = V _{CC} or GND; V _{SW} = GND or V _{CC} ; V _{CC} = 2.7 V			2	μA
ΔI _{CC}	additional supply current	V _I = 2.6 V; V _{SW} = GND or V _{CC} ; V _{CC} = 4.3 V	-	-	10	μA
		V _I = 1.8 V; V _{SW} = GND or V _{CC} ; V _{CC} = 4.3 V	-	-	15	μA
C _I	input capacitance	pins nS	-	1.5	-	pF
C _{S(OFF)}	OFF-state capacitance	pins nY0 and nY1; V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	35	-	pF
C _{S(ON)}	ON-state capacitance	pins nZ; V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	75	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 3.3 V.

11.1 Test circuits

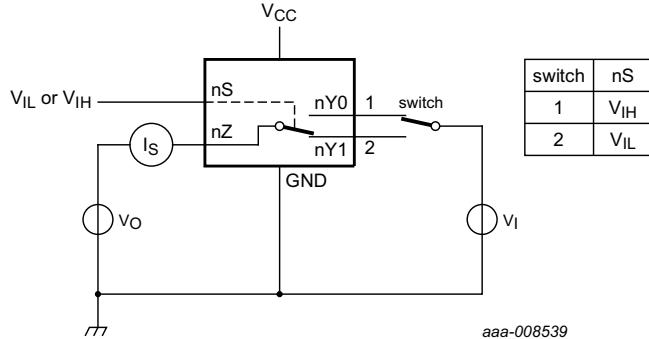


Fig 3. Test circuit for measuring OFF-state leakage current

11.2 ON resistance

Table 8. ON resistance

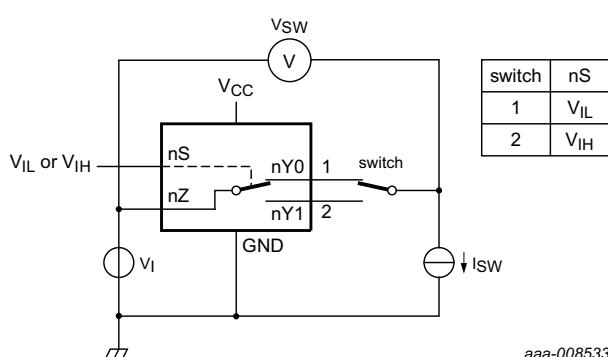
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ ^[1]	Max	
R _{ON}	ON resistance	V _I = V _{CC} –4.5 V to V _{CC} ; I _{SW} = 100 mA; V _{CC} = 2.7 V; see Figure 4	-	0.8	1.3	Ω
R _{ON(flat)}	ON resistance (flatness)	V _I = V _{CC} –4.5 V to V _{CC} ; I _{SW} = 100 mA; V _{CC} = 2.7 V; see Figure 4	-	0.3	-	Ω
ΔR _{ON}	ON resistance mismatch between channels	V _I = V _{CC} –4.5 V; I _{SW} = 100 mA; V _{CC} = 2.7 V; see Figure 4	-	0.1	-	Ω

[1] Typical values are measured at T_{amb} = 25 °C.

[2] Measured at identical V_{CC}, temperature and input voltage.

11.3 ON resistance test circuit and graphs



$$R_{ON} = V_{SW} / I_{SW}.$$

Fig 4. Test circuit for measuring ON resistance

12. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			Unit
			Min	Typ ^[1]	Max	
t_{en}	enable time	nS to nZ; see Figure 5				
		$V_{CC} = 2.7\text{ V}$ to 3.6 V	[2]	-	80	160
		$V_{CC} = 3.6\text{ V}$ to 4.3 V	[3]	-	70	120
t_{dis}	disable time	nS to nZ; see Figure 5				
		$V_{CC} = 2.7\text{ V}$ to 3.6 V	[2]	-	25	50
		$V_{CC} = 3.6\text{ V}$ to 4.3 V	[3]	-	25	50
t_{b-m}	break-before-make time	see Figure 6		[4]		
		$V_{CC} = 2.7\text{ V}$ to 3.6 V		15	55	-
		$V_{CC} = 3.6\text{ V}$ to 4.3 V		12	45	-

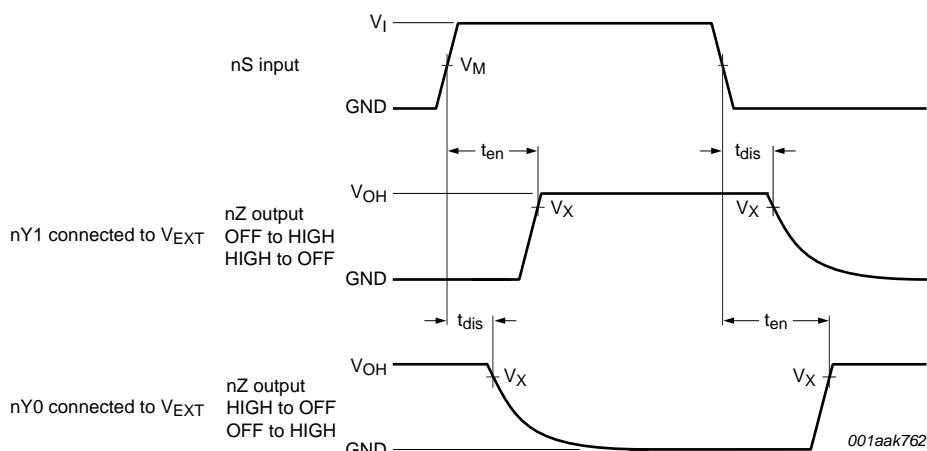
[1] Typical values are measured at $T_{amb} = 25^{\circ}\text{C}$.

[2] Typical values are measured at $V_{CC} = 3.3\text{ V}$.

[3] Typical values are measured at $V_{CC} = 4.3\text{ V}$.

[4] Guaranteed by design.

12.1 Waveform and test circuits



Measurement points are given in [Table 10](#).

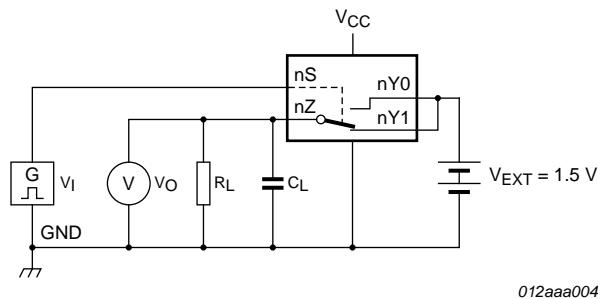
Logic level: V_{OH} and V_{OL} are typical output voltage levels that occur with the output load.

Fig 5. Enable and disable times

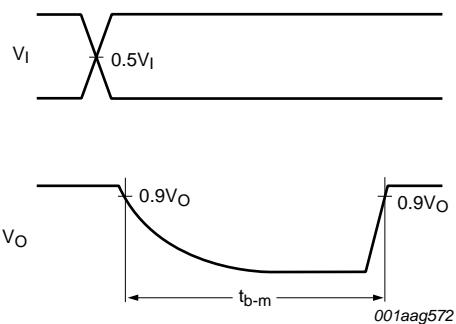
Table 10. Measurement points

Supply voltage	Input	Output	
V_{CC}	V_M	V_I	V_X

2.7 V to 4.3 V $0.5V_{CC}$ V_{CC} $0.9V_{OH}$

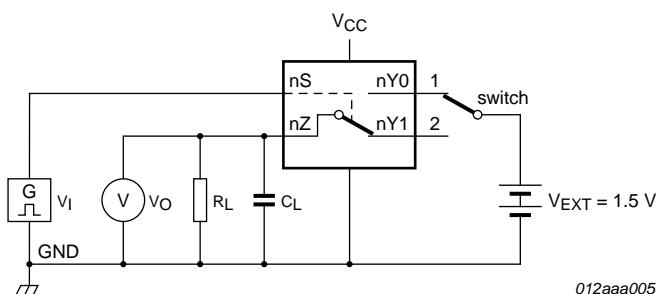


a. Test circuit.



b. Input and output measurement points

Fig 6. Test circuit for measuring break-before-make timing

Test data is given in [Table 11](#).

Definitions test circuit:

 R_L = Load resistance. C_L = Load capacitance including jig and probe capacitance. V_{EXT} = External voltage for measuring switching times.

Fig 7. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Input	Load		
V_{CC}	V_I	t_r, t_f	C_L	R_L
2.7 V to 4.3 V	V_{CC}	≤ 2.5 ns	35 pF	50 Ω

12.2 Additional dynamic characteristics

Table 12. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $V_I = \text{GND}$ or V_{CC} (unless otherwise specified); $t_f = t_{fI} \leq 2.5 \text{ ns}$; $T_{amb} = 25^\circ\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	$f_i = 20 \text{ Hz to } 20 \text{ kHz}$; $R_L = 32 \Omega$; see Figure 8				
		$V_{CC} = 2.7 \text{ V}$; $V_I = 2 \text{ V}$ (p-p)	-	0.07	-	%
		$V_{CC} = 4.3 \text{ V}$; $V_I = 2 \text{ V}$ (p-p)	-	0.03	-	%
$f_{(-3\text{dB})}$	-3 dB frequency response	$R_L = 50 \Omega$; see Figure 9				
		$V_{CC} = 2.7 \text{ V to } 4.3 \text{ V}$	-	100	-	MHz
α_{iso}	isolation (OFF-state)	$f_i = 100 \text{ kHz}$; $R_L = 50 \Omega$; see Figure 10				
		$V_{CC} = 2.7 \text{ V to } 4.3 \text{ V}$	-	-60	-	dB
Xtalk	crosstalk	between switches; $f_i = 100 \text{ kHz}$; $R_L = 50 \Omega$; see Figure 11				
		$V_{CC} = 2.7 \text{ V to } 4.3 \text{ V}$	-	-60	-	dB
Q_{inj}	charge injection	$f_i = 1 \text{ MHz}$; $C_L = 0.1 \text{ nF}$; $R_L = 1 \text{ M}\Omega$; $V_{gen} = 0 \text{ V}$; $R_{gen} = 0 \Omega$; see Figure 12				
		$V_{CC} = 2.7 \text{ V}$	-	3	-	pC
		$V_{CC} = 3.3 \text{ V}$	-	4	-	pC
		$V_{CC} = 4.3 \text{ V}$	-	5	-	pC

12.3 Test circuits

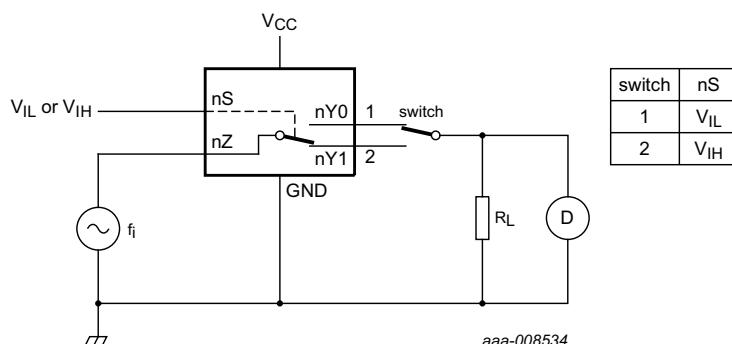
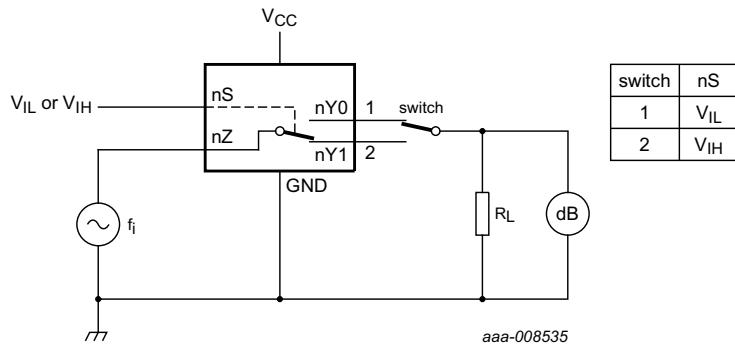
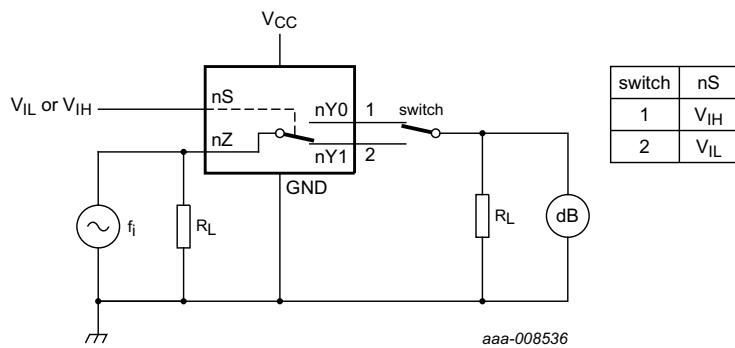


Fig 8. Test circuit for measuring total harmonic distortion



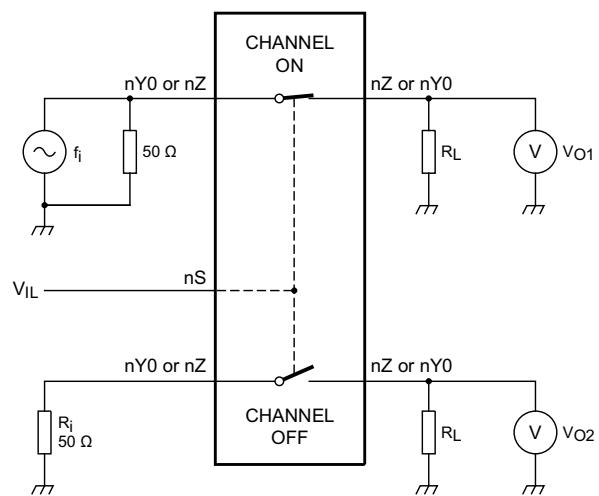
Adjust f_i voltage to obtain 0 dBm level at output. Increase f_i frequency until dB meter reads -3 dB.

Fig 9. Test circuit for measuring the frequency response when channel is in ON-state



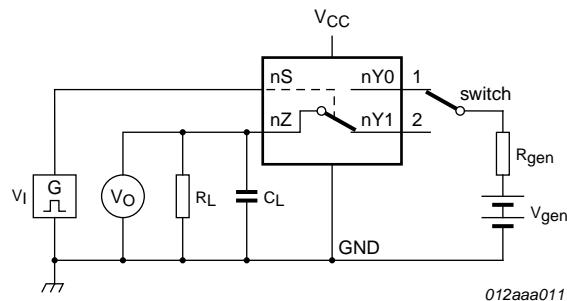
Adjust f_i voltage to obtain 0 dBm level at input.

Fig 10. Test circuit for measuring isolation (OFF-state)

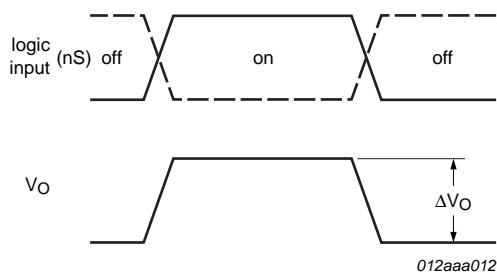


$20 \log_{10} (V_{O2} / V_{O1})$ or $20 \log_{10} (V_{O1} / V_{O2})$.

Fig 11. Test circuit for measuring crosstalk between switches



a. Test circuit



b. Input and output pulse definitions

Definition: $Q_{inj} = \Delta V_O \times C_L$.

ΔV_O = output voltage variation.

R_{gen} = generator resistance.

V_{gen} = generator voltage.

Fig 12. Test circuit for measuring charge injection

13. Package outline

XQFN10: plastic, extremely thin quad flat package; no leads;
10 terminals; body 1.40 x 1.80 x 0.50 mm

SOT1160-1

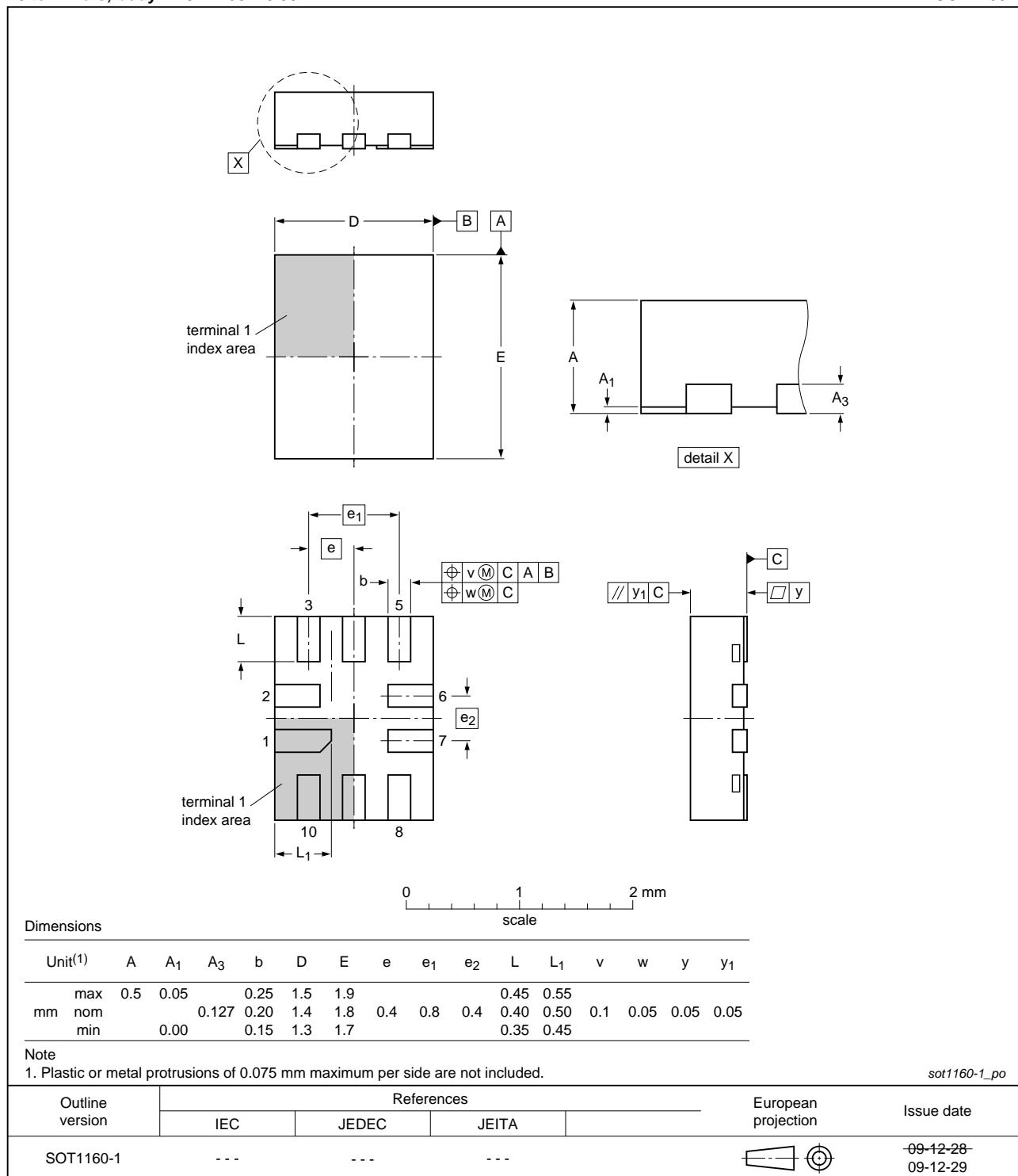


Fig 13. Package outline SOT1160-1 (XQFN10)

14. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX5L2750C v.1	20130906	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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